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Code No: A7707

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech I Semester Examinations, March/April 2011

LOW POWER VLSI DESIGN

(EMBEDDED SYSTEMS AND VLSI DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions

All questions carry equal marks

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1.a) What are the different technical parameter issues connected with VLSI Low Power, Low Voltage design? Explain.

b) What are the advantages of SOI technology? [6+6]

2.a) What are the design considerations for Base, Emitter and collector is the case of B_iCMOS design? Explain.

b) How isolation in BiCMOS structures is carried out? Explain. [6+6]

3.a) What are the considerations for Integrated Analog / Digital BiCMOS process? Explain.

b) With the help of neat sketches explain about Analog / Digital BiCMOS process. [6+6]

4.a) Explain about BSIM3, version 3 current Model.

b) Draw the circuit showing the noise current sources in the electrical schemes of the MOS transistors. [6+6]

5.a) Draw the cross sectional view of the hybrid mode LDD PMOS device and explain about the same.

b) What is the impact of short channel effects on the classical threshold voltage model? Explain. [6+6]

6.a) Draw the circuit for High – performance complementary coupled B_iCMOS circuit of three input NAND gate and explain its working.

b) Draw the circuit for A B_1CMOS buffer using a lateral parasitic pnp BJT in a PMOS structure and explain its working. [6+6]

7.a) Draw a R+N type BiCMOS logic gate circuit and explain its working.

b) Explain about high Beta BiCMOS digital circuits. [6+6]

8. Write notes on any two.
   a) Low Power Latches
   b) Quality measures for Flip-Flops.
   c) HSPICB level 50 Model. [6+6]

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